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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,739	01/16/2002	Matthew M. Borg	10010697	8645

57299 7590 02/09/2006

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EXAMINER	
QUIETT, CARRAMAH J	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,739	BORG, MATTHEW M.	
	Examiner	Art Unit	
	Carramah J. Quiett	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 15-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2* is/are allowed.

6)☒ Claim(s) *1,3-6 and 14-20* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/14/2005 has been entered.

Response to Amendment

2. The amendment(s), filed on 12/14/2005, have been entered and made of record. Claims 1-6 and 14-21 are pending.

3. Applicant's arguments, see Remarks – page 5, filed 12/14/2005, with respect to claims 1 and 2 have been fully considered and are persuasive. The 35 USC 112 rejection of claims 1 and 2 has been *withdrawn*.

4. The indicated allowability of **claim 4** is withdrawn in view of the newly discovered reference(s) to Fowler (U.S. Pat. #6,424,375) in view of Suzuki (U.S. Pat. #6,002,123). Rejections based on the newly cited reference(s) follow.

Response to Arguments

5. Applicant's arguments with respect to claims 1-6 and 14 have been considered but are moot in view of the new ground(s) of rejection.

The Examiner recognizes the Merrill reference (U.S. Pat. #6,833,871) was omitted from the PTO-892 in the previous office action. Although the Merrill reference is not being used in

the present office action, U.S. Pat. #6,833,871 has been included on the present PTO-892. Appropriate correction has been granted.

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. **Claims 1, 3-6, and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fowler (U.S. Pat. #6,424,375) in view of Suzuki (U.S. Pat. #6,002,123).

For **claim 1**, Fowler discloses an image capture system (fig. 1) comprising,

- a plurality of rows of pixels (col. 3, lines 22-32)*, each row comprising:
  - a reset line for providing a reset signal (col. 3, lines 22-32; col. 3, lines 55-58; col. 4, lines 20-22 and 31-67)*;
  - a plurality of pixels (col. 3, lines 22-32)*, each pixel (100) comprising:
  - a first FET (108) having a gate terminal (109) coupled to the reset line (col. 3, lines 55-58; col. 4, lines 20-22 and 31-67), a drain terminal (113) coupled to a supply voltage (V_{dd}; col. 4, lines 25-27), and a source terminal (111) coupled to a readout node (V_{pd}; 110; col. 3, lines 39-42 and col. 4, lines 21-29) ; and
  - a photodetector coupled (112) between a first ground and the readout node (V_{pd}; 110; col. 3, lines 39-42 and col. 4, lines 21-29);
- a switching device (122) selectively coupled to one of the reset lines in the rows of pixels (col. 3, lines 22-32; col. 4, lines 30-34); and

- a reference voltage source (V_{pr}) coupled between a second ground and one of the reset lines via the switching device (col. 4, lines 7-19), wherein the reference voltage source generates a reset voltage (V_g; col. 4, lines 15-19) (col. 4, lines 7-19) and the first and second grounds have the same potential (col. 7, line 61-66).

However, Fowler does not expressly teach that the reference voltage source generates a reset voltage that is independent of the supply voltage. In the same field of endeavor, Suzuki teaches that the reference voltage source generates a reset voltage that is independent of the supply voltage (figs. 1-4; col. 3, line 45 –col. 4, line 23 and col. 4, lines 40-52). In light of the teaching of Suzuki, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the sensor of Fowler with a reference voltage source which generates a reset voltage that is independent of the supply voltage in order to prevent blooming thereby expanding the image sensor's dynamic range (Suzuki, col. 4, lines 31-39).

***Note:** Fowler incorporates a reference that teaches the plurality of row of pixels and a reset line as claimed above. That particular reference was provided in the previous Office Action.

For **claim 3**, Fowler, as modified by Suzuki, further discloses an image capture system wherein the first FET further comprises an n-channel enhancement mode MOSFET (Fowler, col. 3, line 60).

For **claim 4**, Fowler, as modified by Suzuki, further discloses an image capture system wherein the reset voltage is greater than the supply voltage (Suzuki, figs. 3-4; col. 4, lines 40-52).

For **claim 5**, Fowler, as modified by Suzuki, further discloses an image capture system comprising a second FET (114) having a gate terminal coupled to the readout node (V_{pd}; 110) and a drain terminal coupled to the supply voltage. In fig. 1, Fowler illustrates circuits 102 and 104, the drain terminal of second FET (114) is connected to the supply voltage, V_{dd}, and the gate terminal is connected to the first FET (108) via a node (110). Also read Fowler, col. 3, lines 39-43.

For **claim 6**, Fowler, as modified by Suzuki, further discloses an image capture system comprising a third FET (116) having a gate terminal coupled to a row select line, a source terminal coupled to a column line, and a drain terminal coupled to a source terminal of the second FET. See Fowler, figure1 and read col. 3, lines 39-43. The pixel of Fowler is a typical CMOS Active Pixel Sensor (APS) (col. 3,lines 21-54). Therefore, it is inherent for the transistor (116) to have a row select line at the gate terminal and a column line at the source terminal.

For **claim 14**, Fowler, as modified by Suzuki, discloses the image capture system wherein the switching device (Fowler, fig. 1, refs. 106 and 122) comprises a multiplexer. The compare module (106) and the switch (122) receive signals from V_r, V_{pr}, or V_g, and the output of V_2 to reset transistor (108). Therefore, the compare module (106) and the switch (122) inherently multiplex signals from V_r, V_{pr}, and V_g.

8. **Claims 15-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhuse et al. (U.S. Pat. #6,133,862) in view of Suzuki (U.S. Pat. #6,002,123).

For **claim 15**, Dhuse discloses a method comprising:

- providing a first reset (V_{reset1}) signal to a row of pixels (col. 6, line 65 – col. 7, line 9), the first reset signal being derived from a reference voltage (col. 7, lines 46-51);
- resetting pixels in the row of pixels (col. 6, line 65 – col. 7, line 9) in response to the first reset signal (V_{reset1}) using a supply voltage, the supply voltage being different from the reference voltage;

  In col. 7, lines 45-51, Dhuse teaches that the sensor array is reset to a value of V_{reset}, which is approximately the supply voltage (V_{reset} approximately V_{cc}-V_{TM1}; col. 5, line 19 – 24);
- reading a first plurality of voltage values generated at the pixels following a light exposure interval (col. 5, line 57 – col. 6, line 1; col. 6, line 65 – col. 7, line 9);
- providing a second reset signal (V_{reset2}) to the row of pixels (col. 6, line 65 – col. 7, line 9), the second reset signal being derived from the reference voltage (col. 7, lines 54-56);
- reading a second voltage value from the pixel (col. 7, lines 56-59); and
- generating a plurality of pixel values using the first and the second pluralities of voltage values (col. 6, line 65 – col. 7, line 9; col. 7, lines 51-54 and 59-67).

However, Dhuse does not teach a reference voltage that is independent of a supply voltage. In the same field of endeavor, Suzuki teaches a reference voltage that is independent of a supply voltage (figs. 1-4; col. 3, line 45 –col. 4, line 23 and col. 4, lines 40-52). In light of the teaching of Suzuki, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the sensor of Dhuse with a reference voltage that is independent

of a supply voltage in order to prevent blooming thereby expanding the image sensor's dynamic range (Suzuki, col. 4, lines 31-39).

For **claim 16**, Dhuse, as modified by Suzuki, further discloses a method wherein the plurality of pixel values equal the corresponding second plurality of voltage values minus the corresponding first plurality of voltage values (Dhuse, col. 7, lines 59-66).

For **claim 17**, Dhuse, as modified by Suzuki, further discloses a method wherein the first plurality of voltage values are approximately proportional to light intensities detected by the pixels during the light exposure interval (Dhuse, col. 5, line 57 – col. 6, line 9).

For **claim 18**, Dhuse, as modified by Suzuki, further discloses a method comprising repeating the providing a first reset signal, reading a first plurality of voltage values, providing a second reset signal, reading, and generating a plurality of pixel values for another row of pixels (Dhuse, col. 7, lines 45-67).

For **claim 19**, Dhuse, as modified by Suzuki, further discloses a method wherein the generating is performed by a column circuit (Dhuse, col. 7, lines 10-35).

For **claim 20**, Dhuse, as modified by Suzuki, further discloses a method wherein the reading a first plurality of voltage values comprises exposing photodiodes to incident light (Dhuse, col. 4, lines 7-22).

Allowable Subject Matter

9. **Claim 2** is allowed.

10. The following is a statement of reasons for the indication of allowable subject matter:

Claim 2 is allowed because the prior art does not teach or fairly suggest the image capture system, comprising: an operational amplifier buffer comprising (1) an output coupled by the switching device to one of the reset lines (2) *a non-inverting input coupled to the reference voltage source to receive the reset voltage, and (3) an inverting input coupled to the output in a feedback loop, wherein the feedback loop does not pass through the readout node.*

11. **Claim 21** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

Claim 21 is allowed because the prior art does not teach or fairly suggest the image capture system of claim 6, further comprising an operational amplifier comprising (1) an output coupled by the switching device to one of the reset lines, *(2) a non-inverting input coupled to the reference voltage source to receive the reset voltage, and (3) an inverting input coupled to the output in a feedback loop, wherein the feedback loop does not pass through the readout node.*

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carramah J. Quiett whose telephone number is (571) 272-7316. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CJQ
February 3, 2006

NGOC-YEN VU
PRIMARY EXAMINER